Project Simulation

Before programming the FPGA, it is recommended to run a simulation to verify if the system is working as expected.

a) Steps to Simulate:

1. Access the Simulate tab in the top menu of ChipInventor.
2. Choose Advanced Simulation or Dynamic Simulation, depending on the desired level of detail.
3. Click Run Iverilog to start the simulation.

b) What to Observe During Simulation:

 CAN Transmission

- Confirm that the tx_request_i signal, coming from the one_hz_clock, triggers periodic transmissions (e.g., every 1 second).
- The tx_o signal should be activated whenever a transmission request occurs, indicating that a CAN frame has been transmitted.

 Status Signals

- transmit_irq_o should be activated whenever a transmission starts (check if LED0 would turn on).
- transmit_ack_irq_o confirms the frame was acknowledged on the bus (represented by LED1).

 Data Reception

- If frames are received (including loopback tests), receive_irq_o will be triggered.
- The uart_can_std_printer should convert the data and send it through the uartTxPin output.
- Verify if txDone signals the end of UART transmission (LED5 would be activated).

c) What to Do in Case of Errors:

If there is no transmission or reception, review the following:

- The connections of tx_request_i, rx_i, and tx_o signals.
- The timing parameters: baud_r_presc_i, time_segment_1_i, time_segment_2_i.

- The configured data: packet_id_i, packet_length_i, and tx_data_i.
- Make sure resets and clocks are correct and that all modules are receiving valid signals.