

# Synthesis and Results

Now, it's time to synthesize your project.

1. Open the **Synthesize tab** to transform the **Verilog code into a physical circuit** representation.

2. The synthesizer will:

- **Check for design errors.**
- **Optimize the circuit to ensure performance and feasibility.**

3. If any issues are found, **adjust the blocks** in the diagram and re-synthesize.

Explore the other ChipInventor pages, such as View and Results, and compare them with your first project to identify potential improvements and enhancements.

---

Revision #4

Created 18 February 2025 18:59:21 by Caroline

Updated 18 February 2025 20:01:37 by Caroline