

Creating Flip-Flop Example

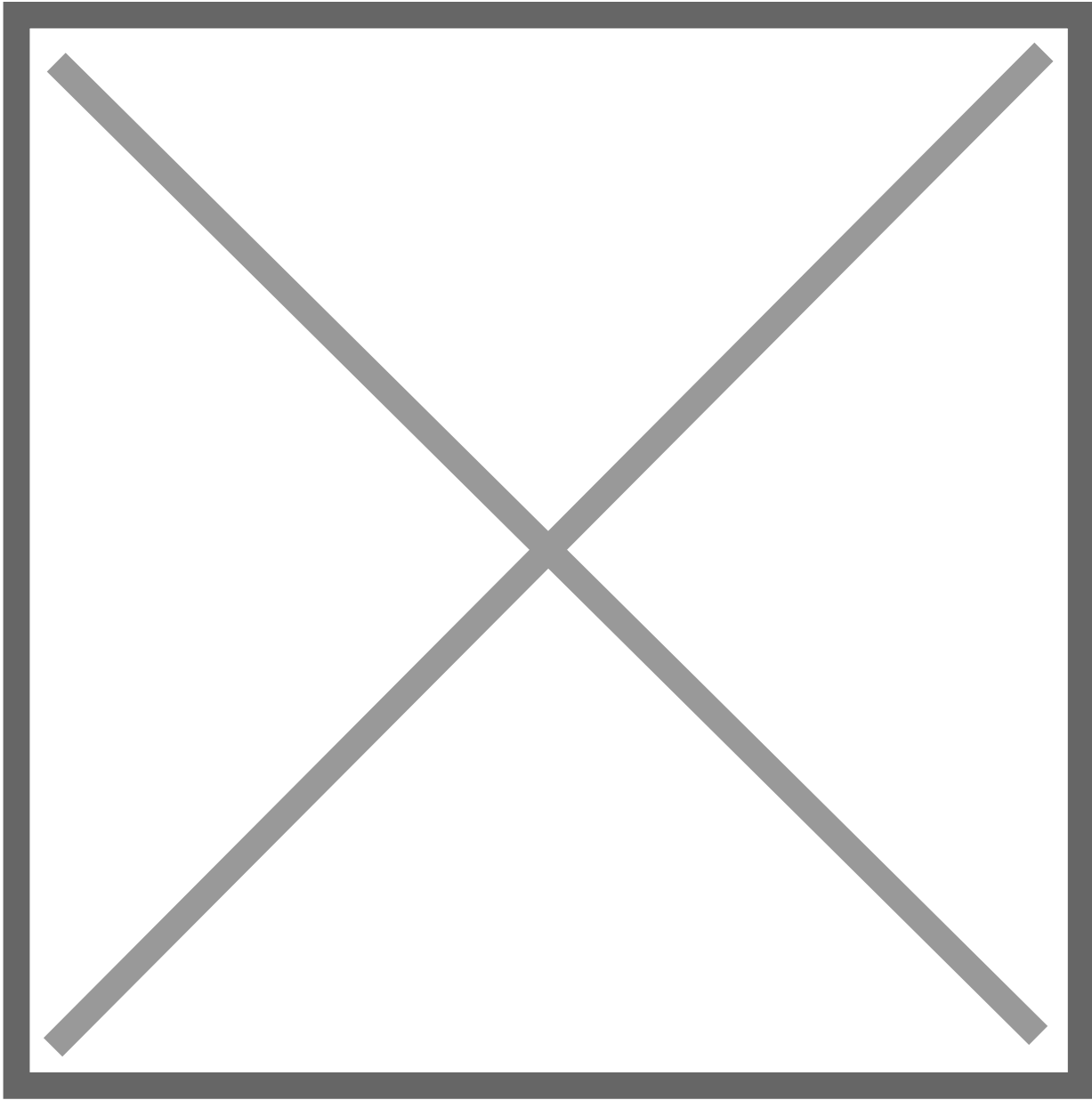
Welcome to our tutorial on TestBenches in ChipInventor. We'll create a simple Flip-Flop circuit to highlight how to set up and run TestBench simulations. Rather than focusing on circuit details, this guide emphasizes verifying behavior and generating waveforms with the TestBench. By the end, you'll know how to efficiently validate digital logic in ChipInventor and be ready for more complex projects.

a. Creating the Flip-Flop Project

1. Click **New Project** in the top menu.
2. Fill the project details:
 - **Name:** FlipFlop TestBench,
 - **Description:** Basic example of how to use testBench in ChipInventor.
 - **Type:** OpenRoad.
3. Click on **Create Chip** to start the project.

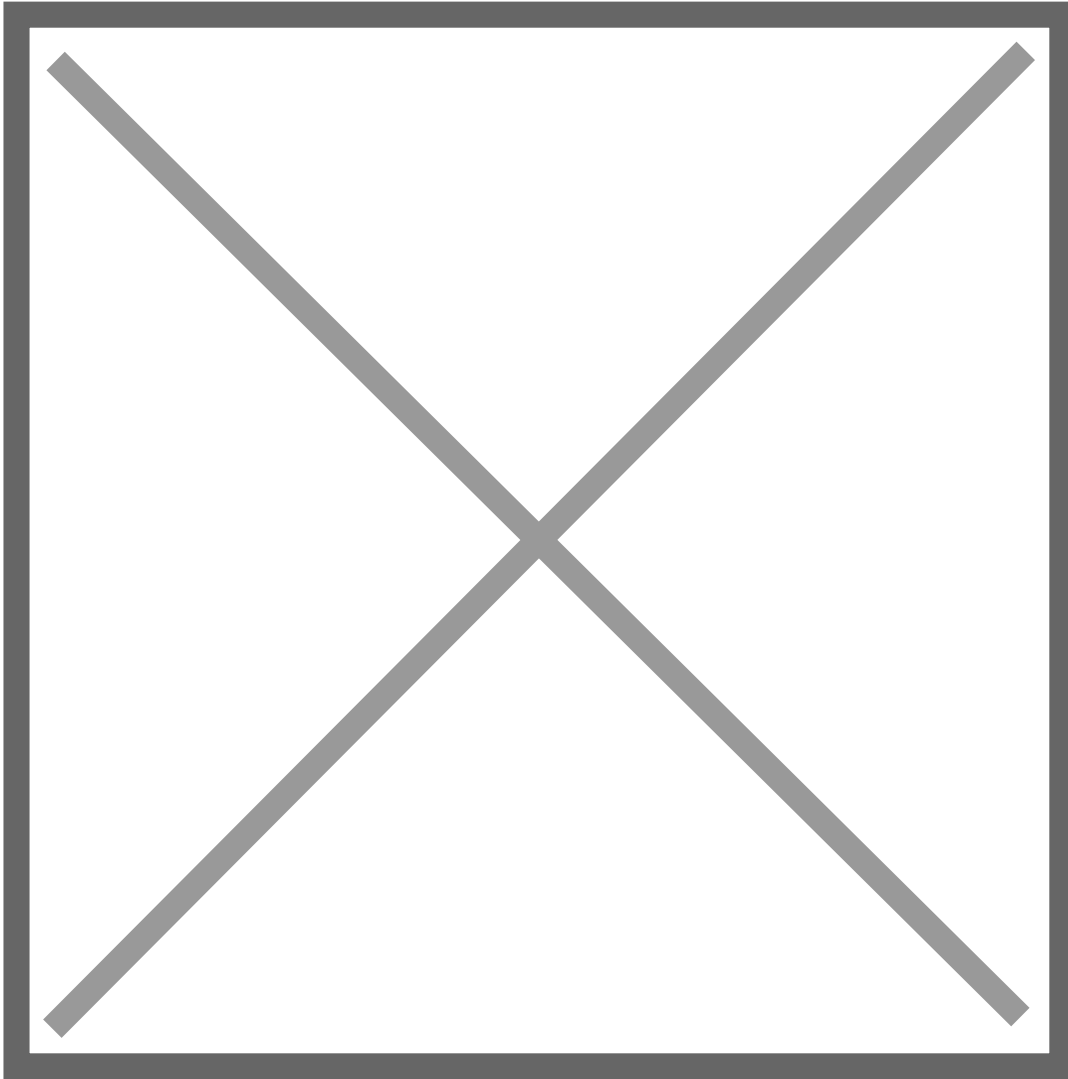
b. Flip-Flop in the Blocks Tab

1. Adding and **Configuring the Flip-Flop**
2. In the Blocks tab, locate the **Flip-Flop D block** and drag it to the workspace.
3. Add three inputs (Inputs) named:
 - **Clock, D, and Reset (names can be customized to facilitate your understanding later).**
4. Add one output (Output) and **name it Q**.



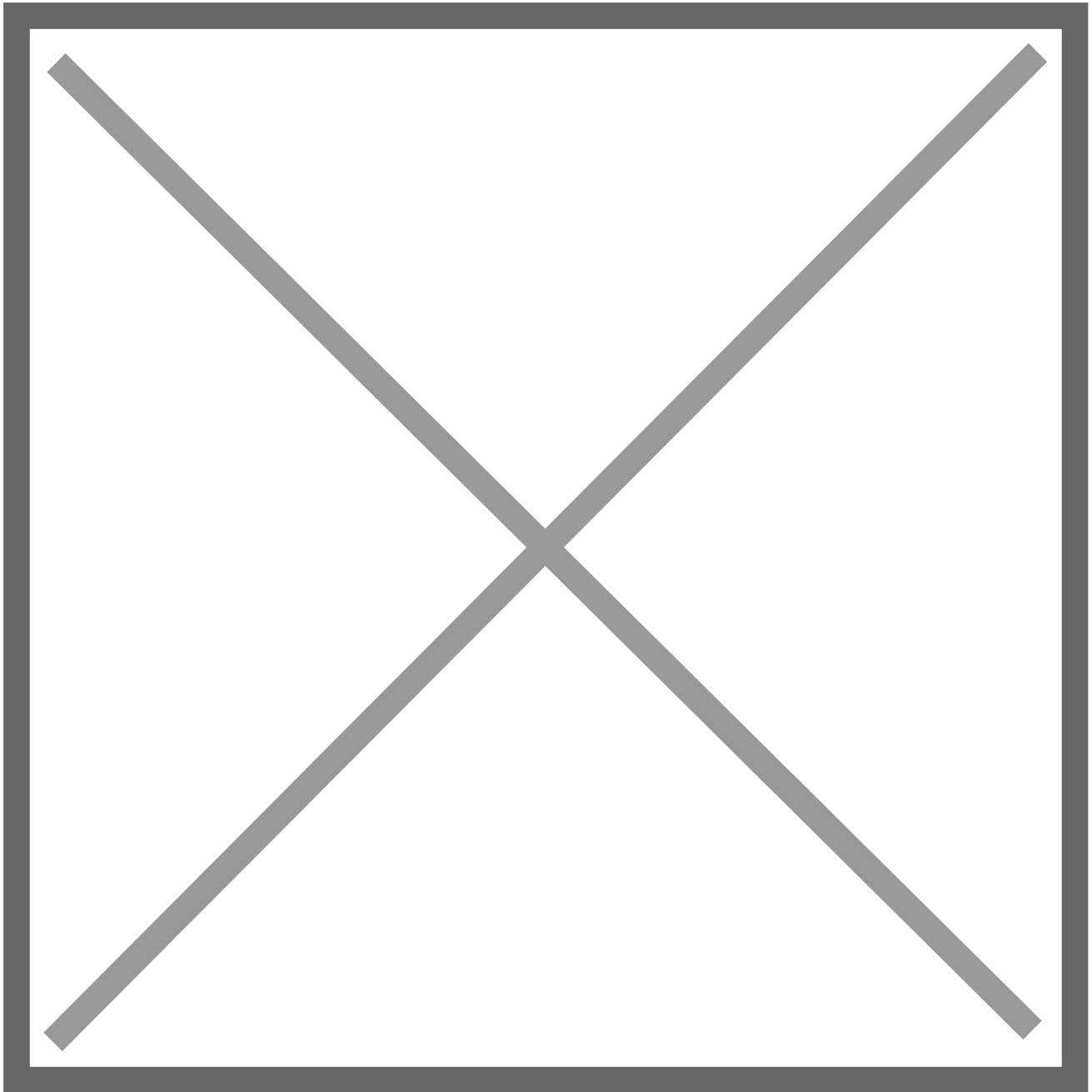
5. Connect the **Clock, D, and Reset input pins** to the respective Flip-Flop inputs.

6. Connect the **Q output pin** to the **output block**.



c. Configuring the TestBench

1. Navigate to the **Simulate tab** in the top menu.
2. Select **Advanced Simulation**.
3. In the side menu, click on **Run Iverilog** to check for potential errors in the generated code.
4. Click on **Create VCD** to generate a file that enables the visualization of circuit signals.
5. Use the integrated viewer to inspect the **Clock, D, Reset, and Q signals**.
6. In the bottom-right corner of the VCD page, click on the **question mark icon to view shortcuts** that can help improve waveform visualization.



d. Improving the TestBench

1. Editing Input Values

- Locate the Verilog code in the left tab.
- Adjust the input signals (for example, changing them from 0 to 1) to test different scenarios.

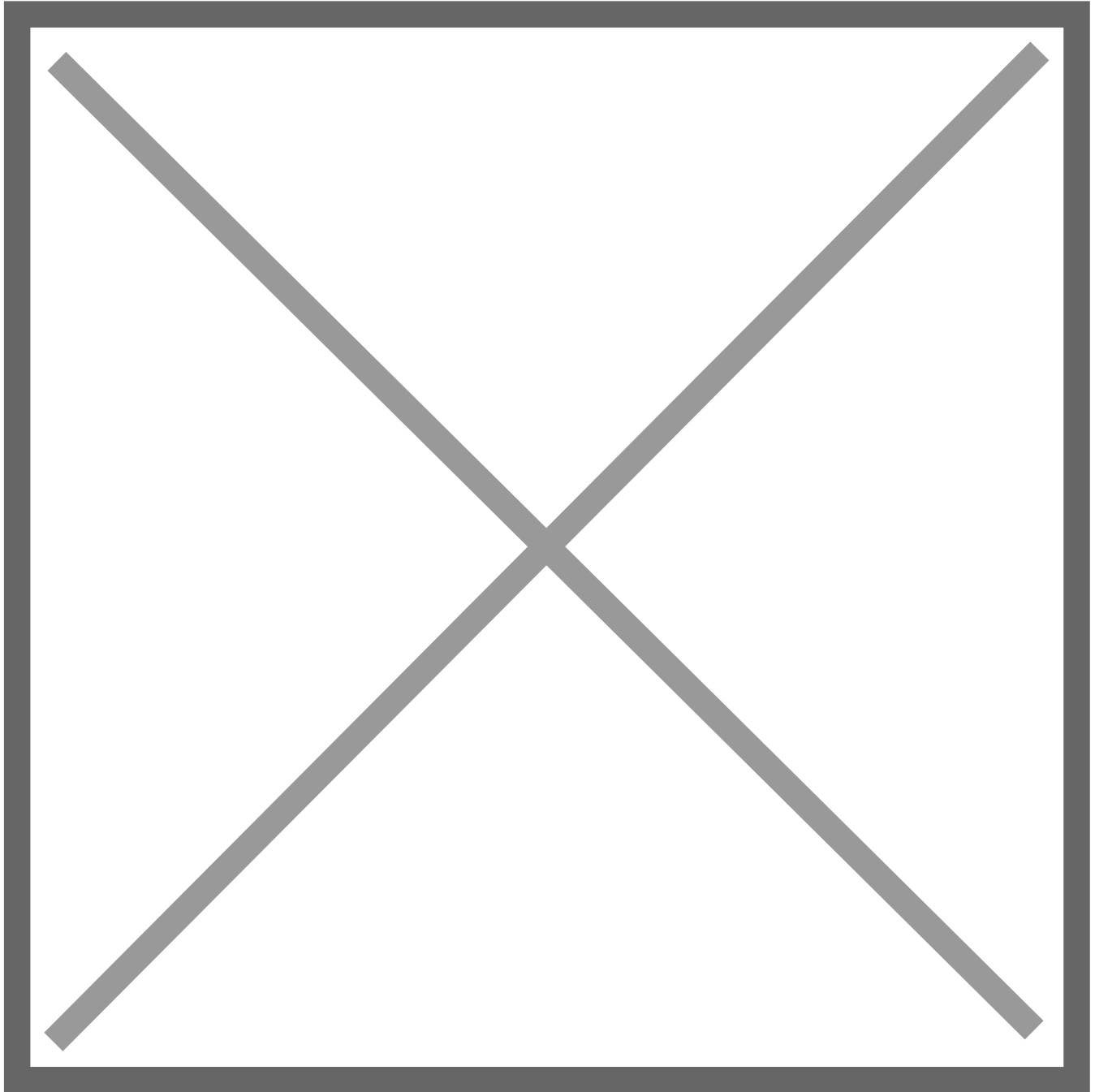
2. Re-running the Simulation

- Click on Menu and select Run Iverilog to compile the changes.
- Click on Create VCD to generate a new waveform file.

3. Understanding the Static TestBench

- The default TestBench includes predefined sequences.
- By manually editing the inputs, you create customized tests to better evaluate the circuit.

If you notice differences in the signals displayed in the newly generated VCD, it means your changes to the TestBench were successfully applied.



e. Analyzing the Results

- Examine the waveforms generated in the viewer.

- Ensure that the Q output responds correctly to the Clock signal and the Reset command.
- Ask yourself: Does the Q output behavior match expectations regarding the clock and reset?

Revision #3

Created 18 February 2025 19:16:58 by Caroline

Updated 18 February 2025 19:26:23 by Caroline