

Running the Simulation

To test the frequency division, follow these steps:

1. Run the TestBench in ChipInventor:

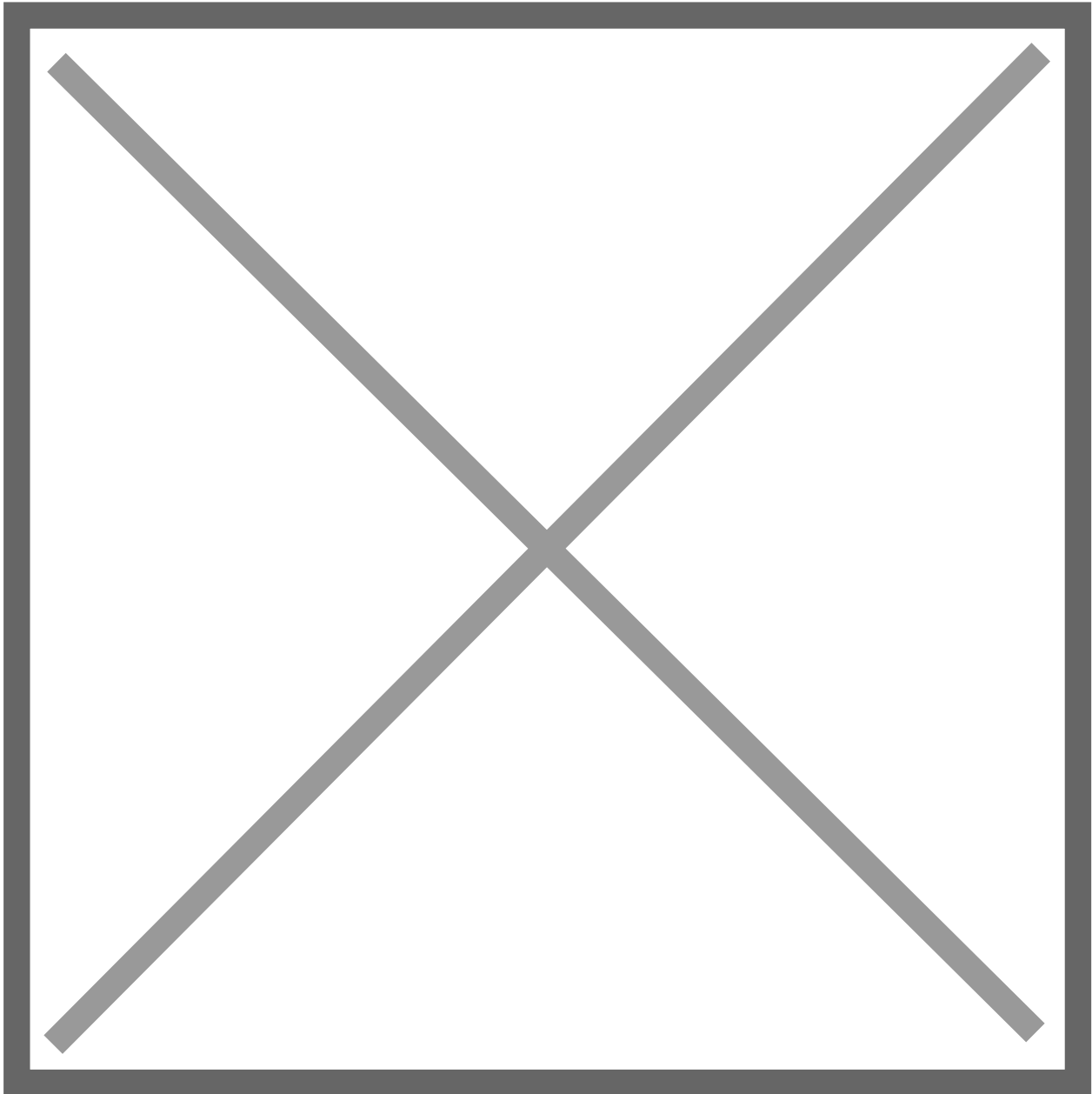
- Click on Menu, after Run Iverilog to compile and execute the simulation.

2. Generate the waveform file:

- Click on Create VCD to create the .vcd file with signal transitions.

3. Open the waveform viewer:

- Inspect b0, Q1, Q2, and led0 to observe how each Flip-Flop divides the input signal frequency.



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