

Fast Fourier Transform (FFT)

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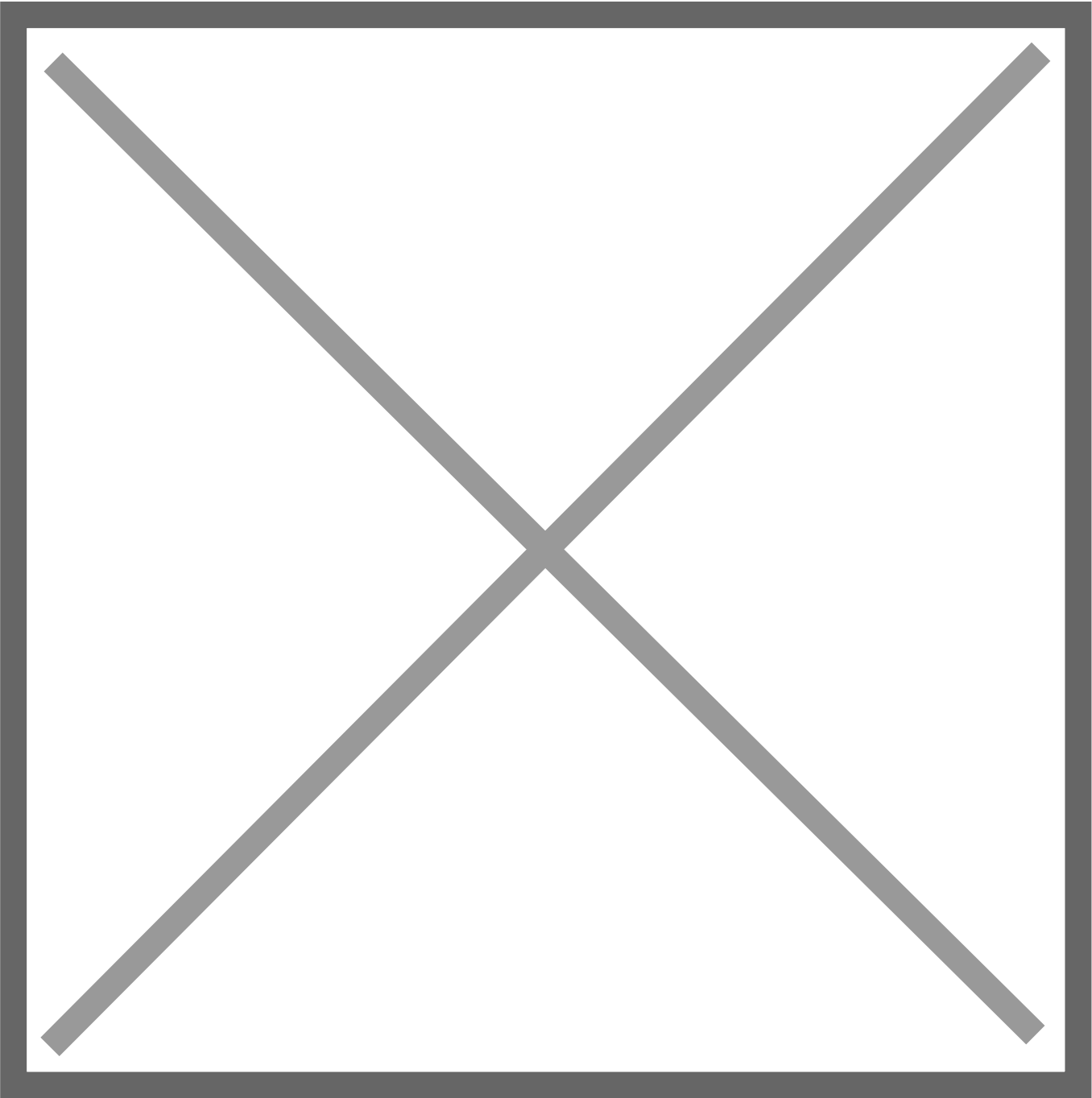
Project Summary

This project implements a 64-point FFT-based audio processing system that captures audio from an INMP441 microphone, processes it, and transmits the results via UART.

Implementation

The design uses Verilog HDL on an FPGA, leveraging a Radix-2² FFT algorithm with single-path delay feedback. It integrates an I2S interface for audio input, a PLL for clock generation (27 MHz to 5.4 MHz), and UART for serial communication at 115200 baud. Key components include pipeline stages for FFT computation, a magnitude calculator, and a data selector for normalized 8-bit output. The system operates synchronously with configurable clock dividers.

Block Diagram



Visual Resources

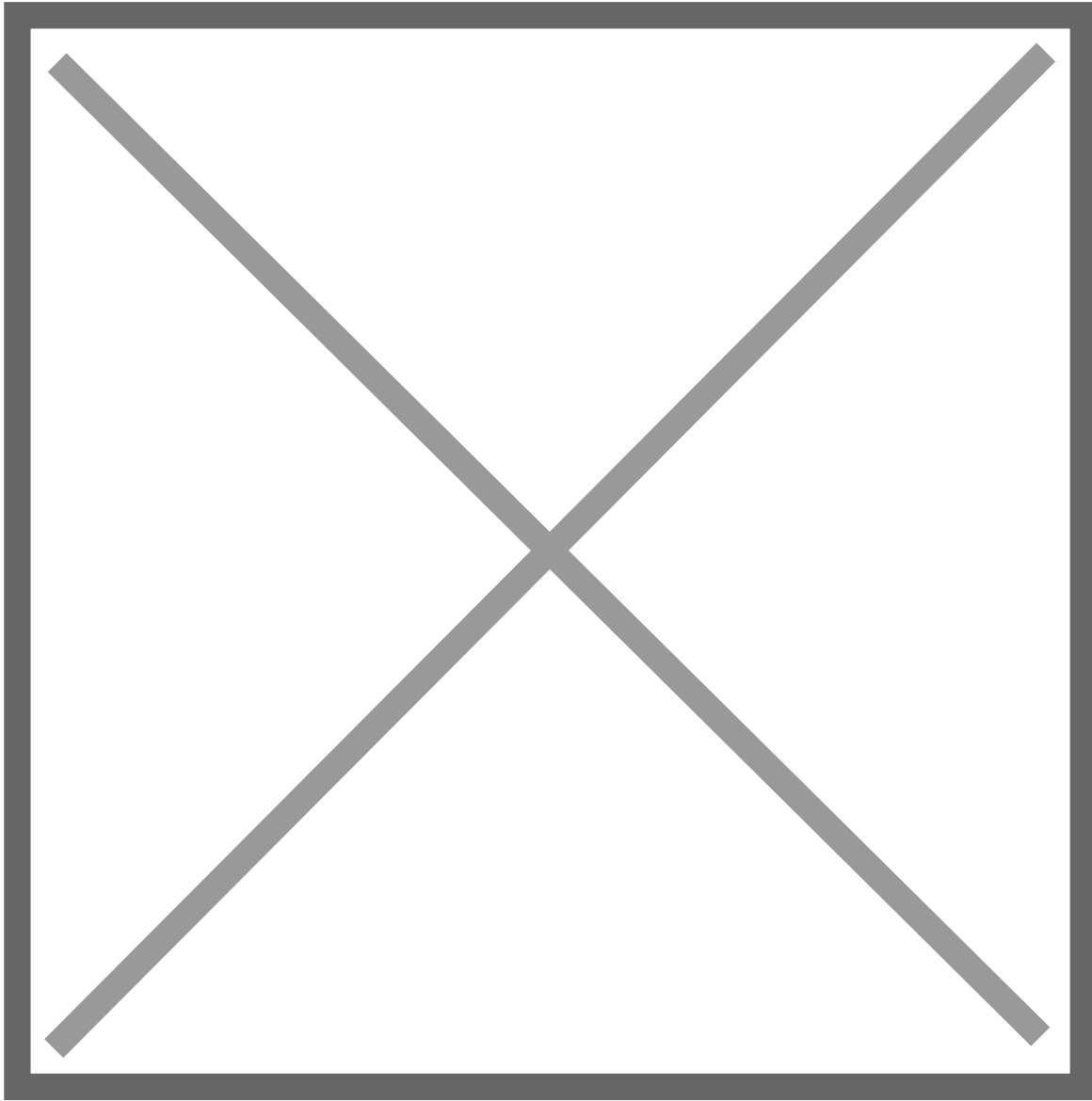


Figure 1: Connections in the FPGA

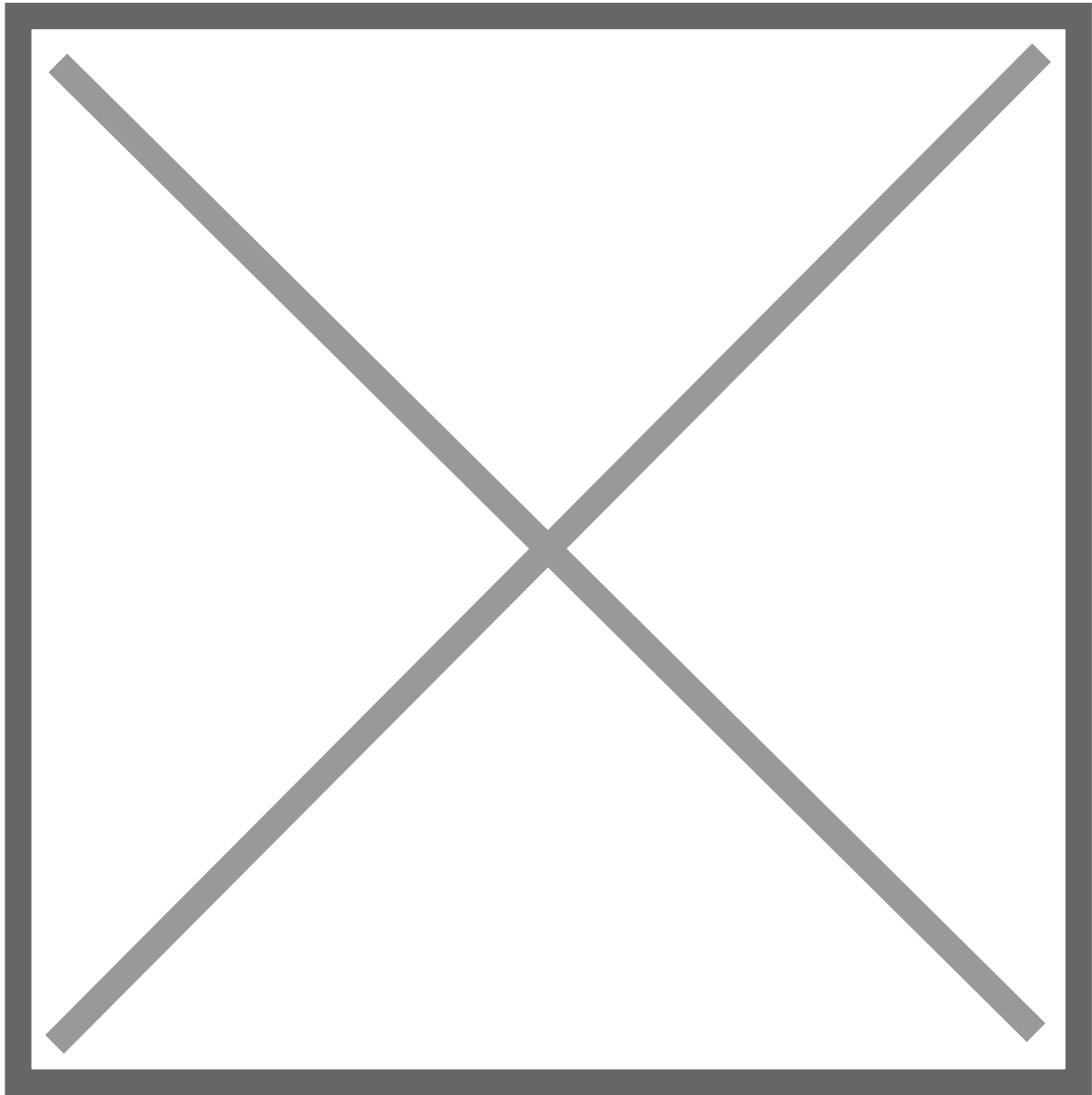


Figure 2: General structure - 64-point FFT

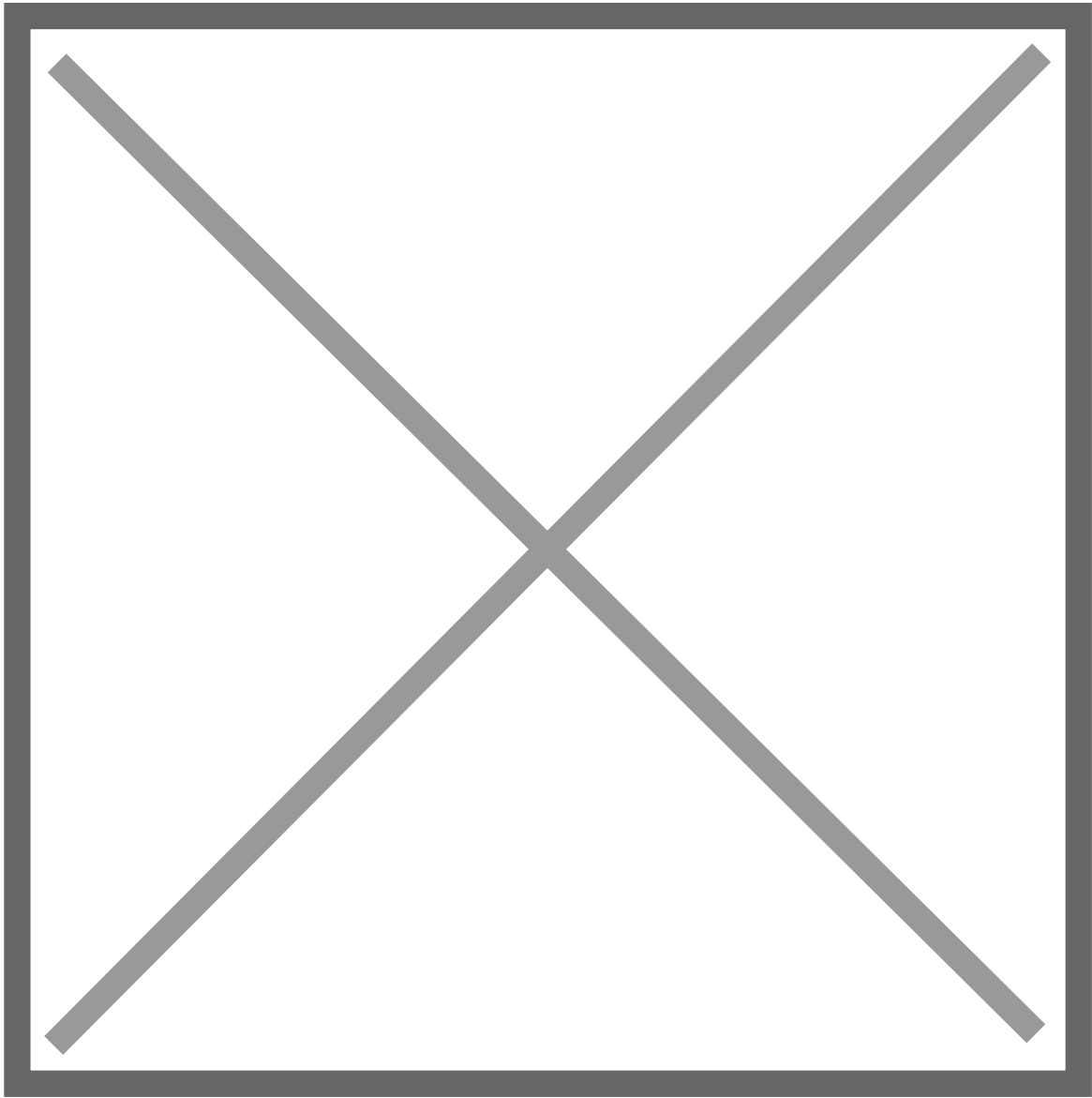


Figure 3: Processing Module

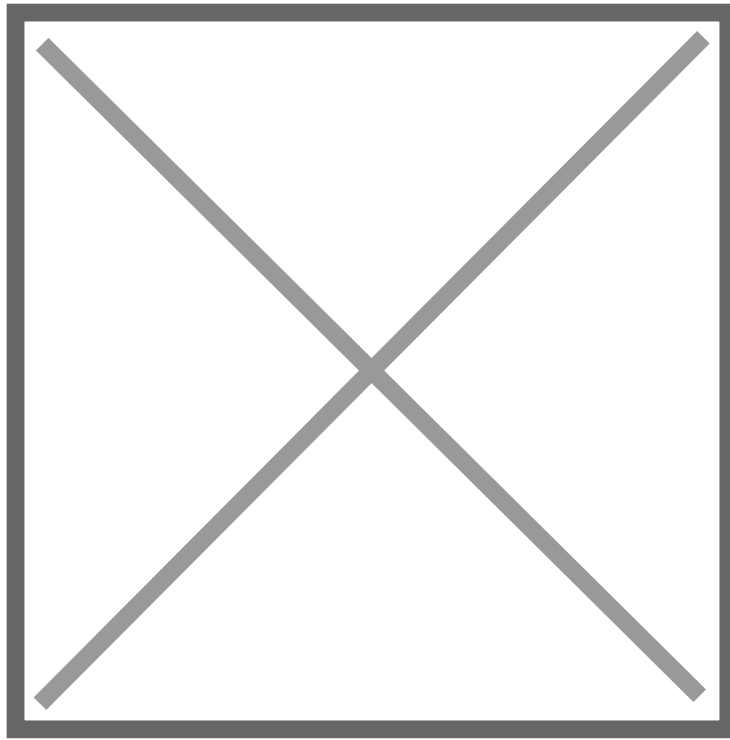


Figure 4: Butterfly-shaped multiplication and addition structure