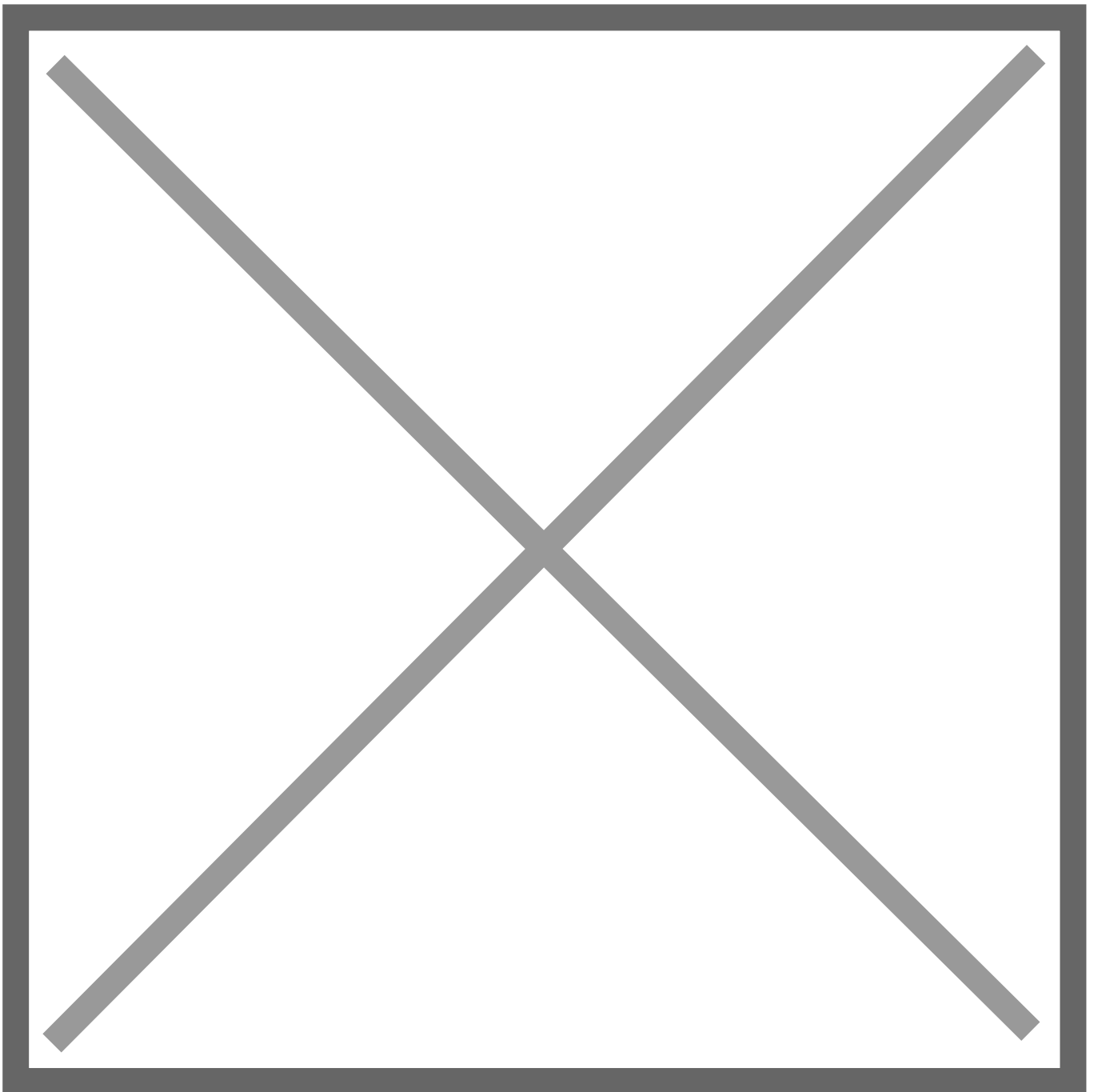


# Implementation

The design uses Verilog HDL on an FPGA, leveraging a Radix-2<sup>2</sup> FFT algorithm with single-path delay feedback. It integrates an I2S interface for audio input, a PLL for clock generation (27 MHz to 5.4 MHz), and UART for serial communication at 115200 baud. Key components include pipeline stages for FFT computation, a magnitude calculator, and a data selector for normalized 8-bit output. The system operates synchronously with configurable clock dividers.

## Block Diagram



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Revision #1

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