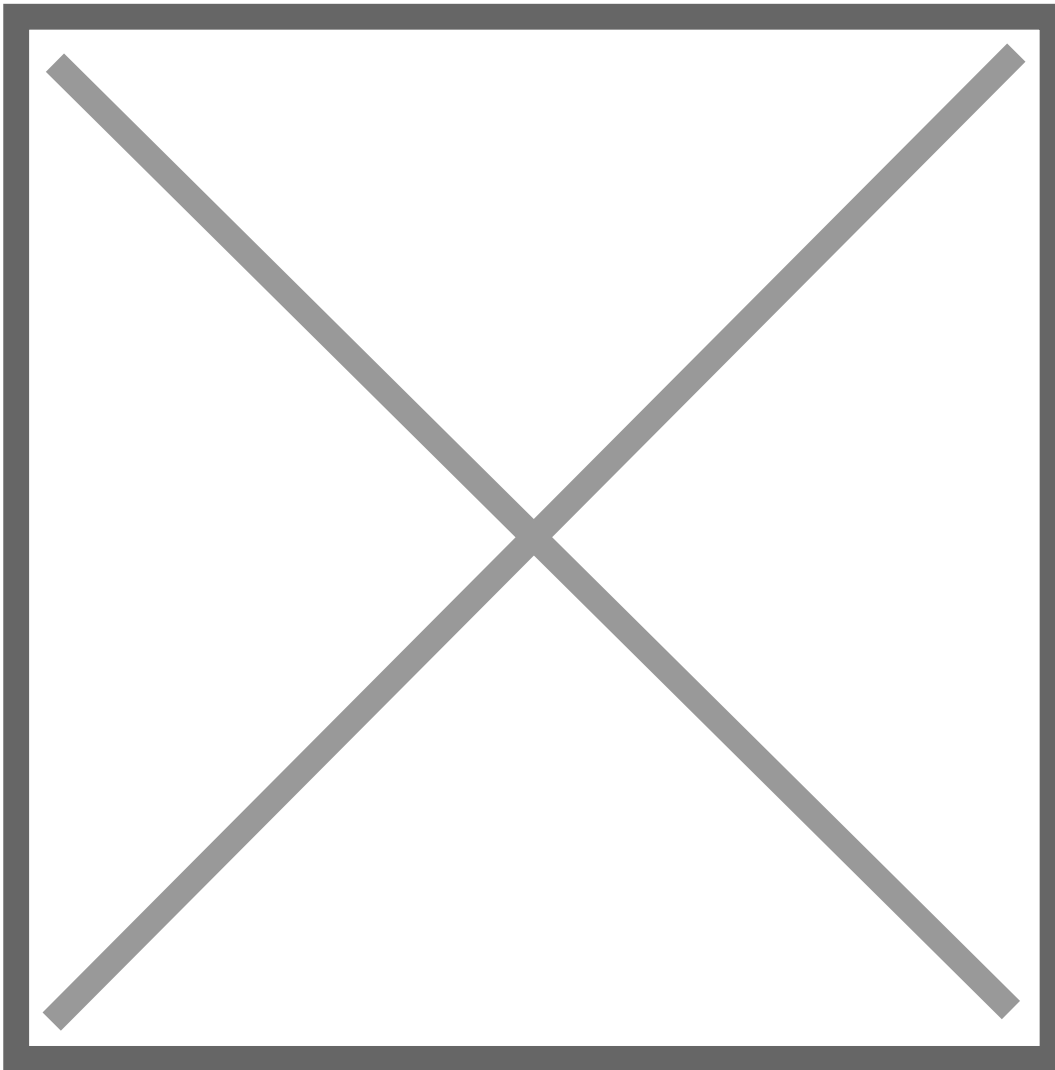


Exploring the Files Page

1. **Now, it's time to automatically generate the Verilog code for your project. On the top navigation bar, click Files. Similar to the Save function, a pop-up will appear to confirm this operation.**



In addition to the Verilog code, the system creates all the files necessary to synthesize your project.

2. **In the Explore section on the left, browse your project files:**
 - Right-click on files to open options.
 - Double-click on the main file to open it in the editor.
3. **Review the Verilog code generated from the Blocks tab diagram.**

- This code translates the blocks into hardware description language.
- For beginners, it's recommended not to modify the code directly.

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