Project Simulation

Before programming the FPGA, simulate the circuit behavior:

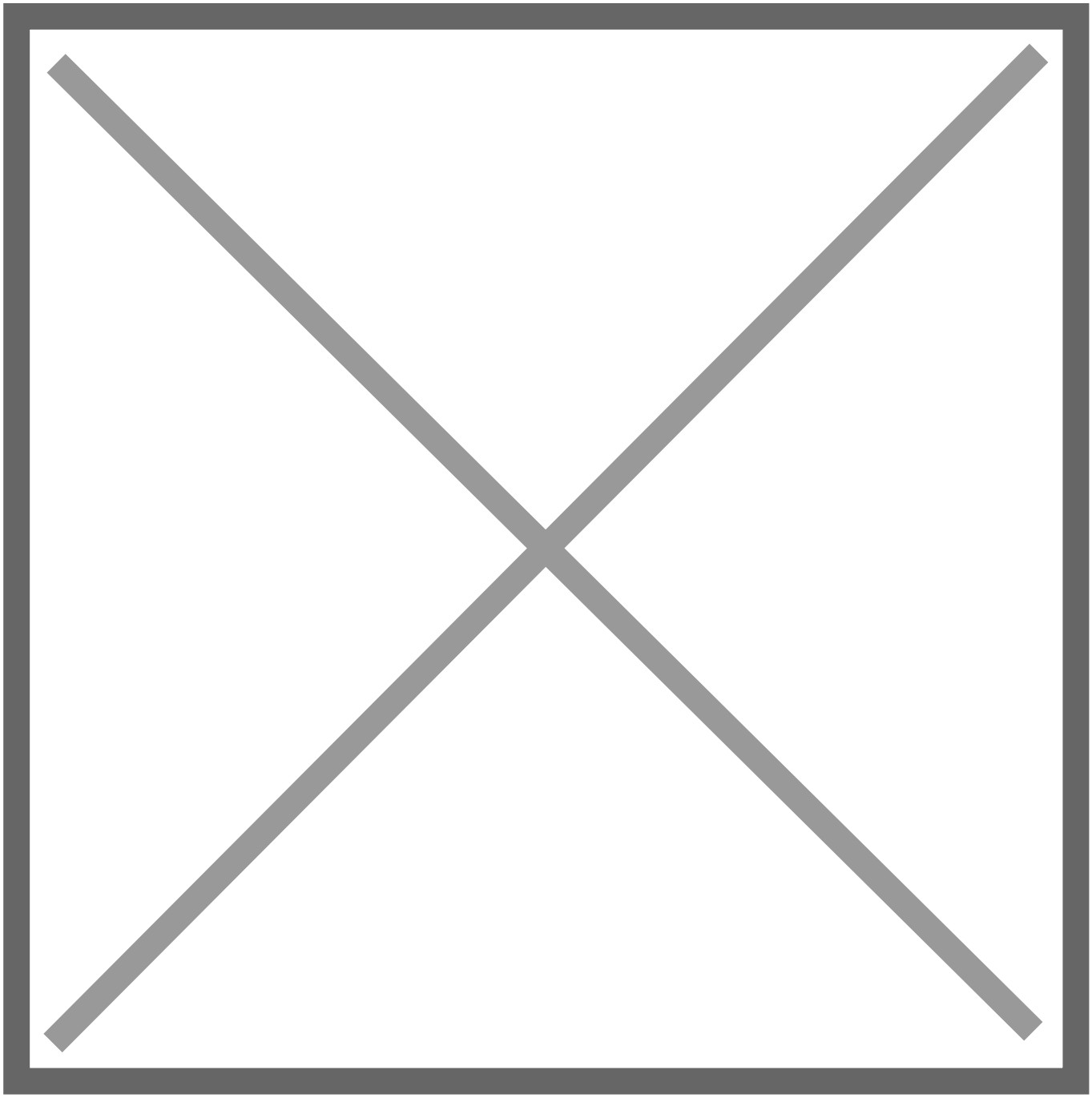
1. Go to the “**Simulate**” tab.

2. Click “**Advanced Simulation**”.

3. In advanced mode, go to **Menu > Run Iverilog**.

4. **Check for messages:**

    - No errors → you're ready for synthesis.
    - Errors → review the block connections and run the simulation again.



During simulation, observe the following signals:

Signal	Description
counter[7:0]	Should increment with each 20 Hz clock pulse.
pwm	PWM signal with increasing duty cycle.
led0	Inverted PWM signal applied to the LED.

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