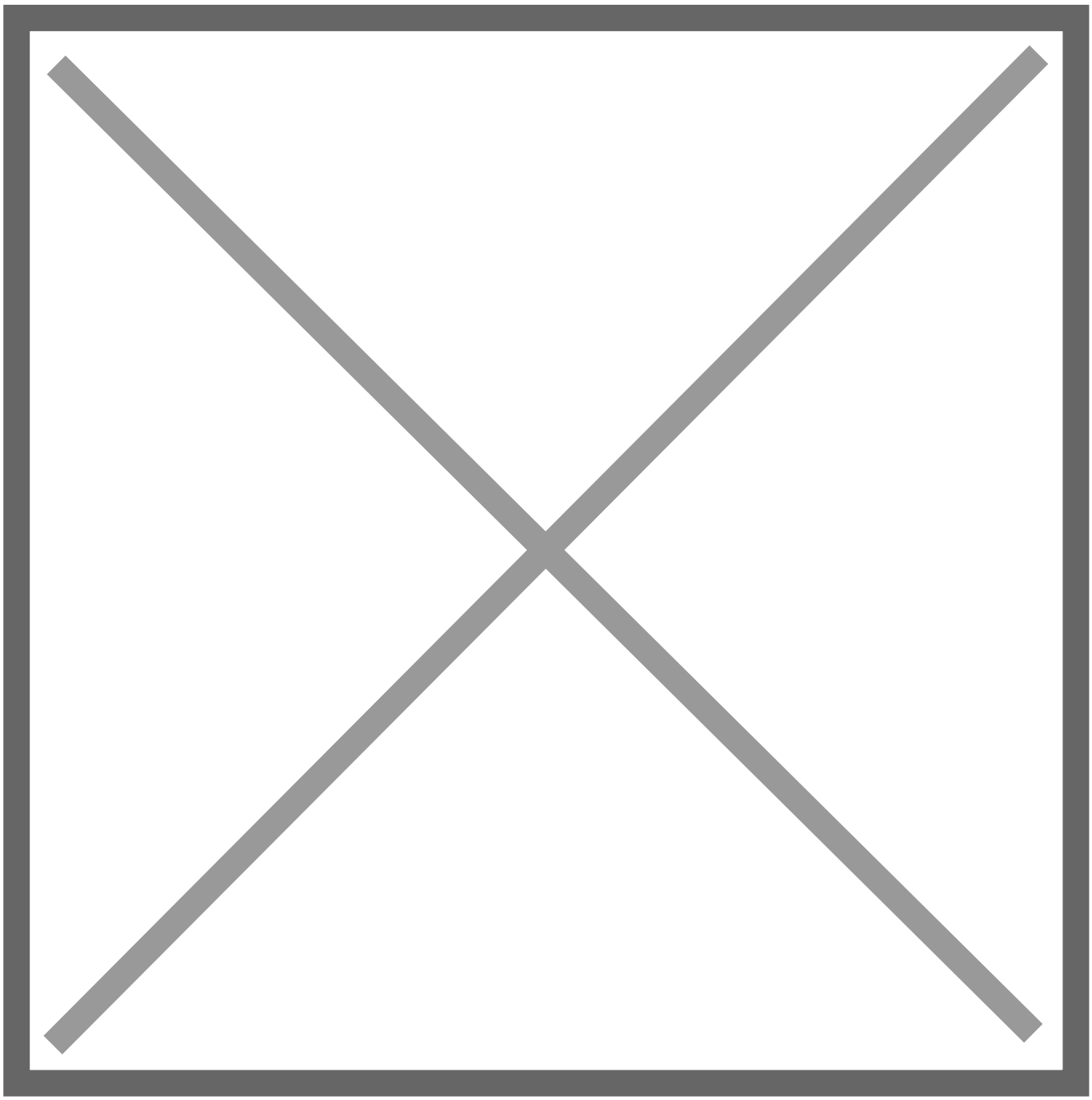
Understanding the Project and the Blocks Used

This project consists of the following blocks:

- **clock_20_hz:** Generates a slower 20 Hz clock from the main FPGA clock. It is used to generate low-frequency pulses.
- **pulse_count_8_bits**: A counter that increments with each 20 Hz clock pulse.
- **pwm_control8:** Generates a PWM signal based on the counter value, with proportional duty cycle.
- **inverterC:** Inverts the PWM signal, acting as final control for the output.
- **Input/Output Pins:**
  - clk: System clock input.
  - l1: Final output with inverted PWM signal (can be connected to an LED).



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