

Reverse Camera

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Project Summary

Implement a rear-view camera system using the Tang Primer 20K FPGA. The project utilizes the capabilities of the ChipInventor Devboard 2.1 to process video input and display a real-time feed, assisting in vehicle reversing maneuvers.

Visual Resources

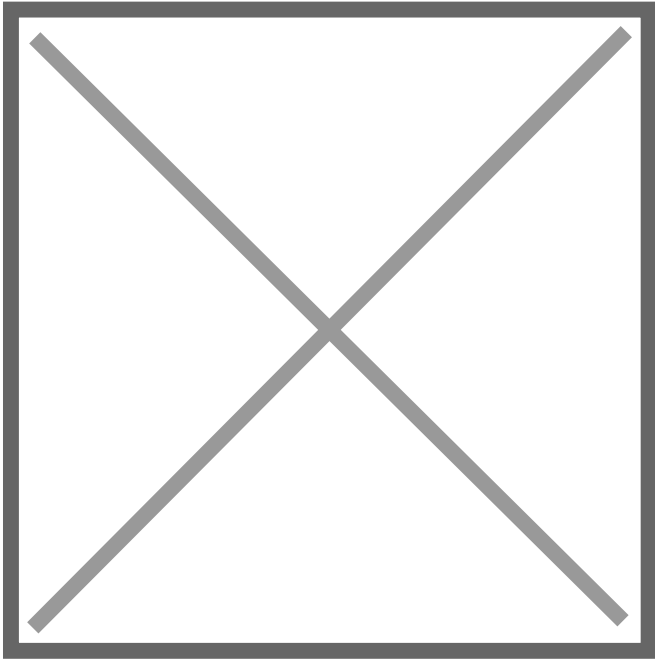


Figure 1: Connections in the FPGA

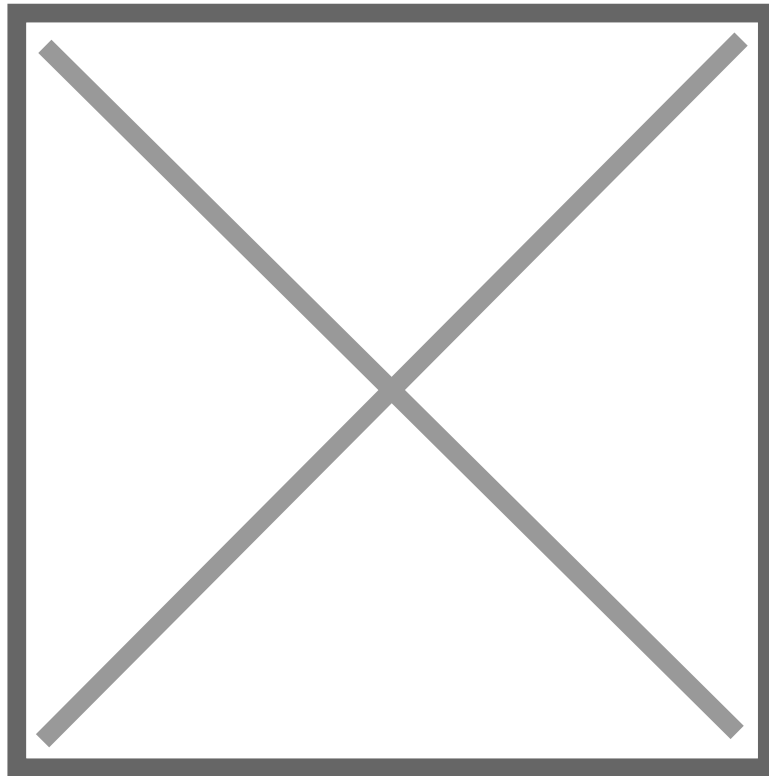


Figure 2: Camera

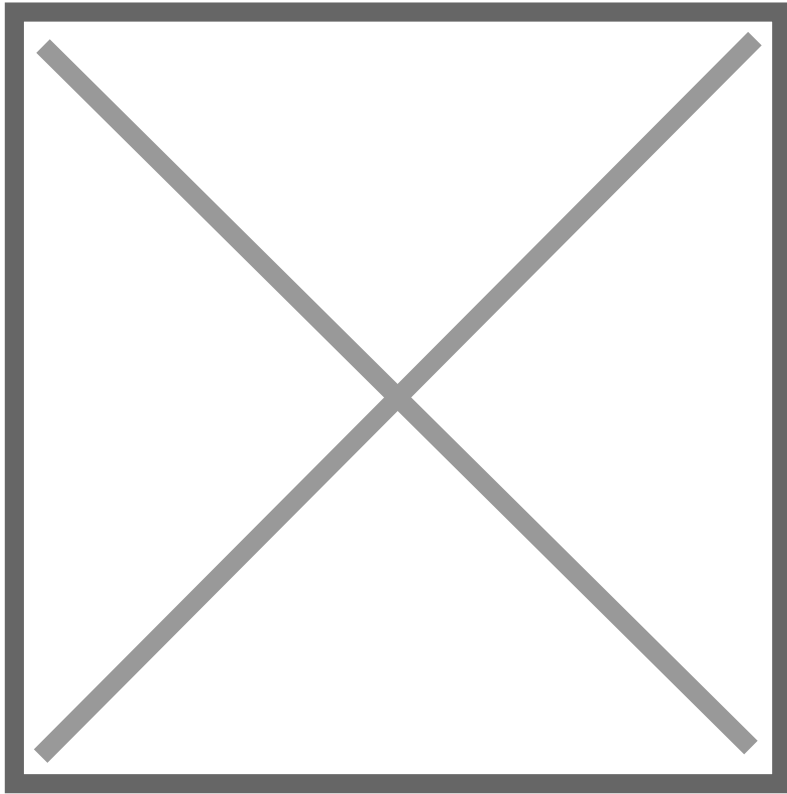


Figure 3: Camera

Implementation

1. About

This rear-view camera system is developed using the ChipInventor platform and implemented on the Tang Primer 20K FPGA. The project integrates a camera module as an input source, processes the video stream in real-time, and outputs the feed to a display.

The FPGA handles video signal processing, overlaying visual guides to assist in parking. Additionally, the system features dynamic trajectory lines that adjust according to the steering angle, providing enhanced maneuverability assistance.

To improve visibility in low-light conditions, a Sobel filter is applied to detect edges, ensuring reliable performance regardless of ambient lighting.

2. Components

- Tang Primer 20k;
- Display TFT 480x272;
- Camera OV5640;
- Sensor HC SR04;

3. Flow Logic

The logical flow begins with the main clock being adjusted by PLLs to 72 MHz, 24 MHz, and 9 MHz. 8-bit data from the OV5640 camera enters through pins, is converted to 16 bits (RGB565), and is configured via I2C using predefined instructions. The video is sent to a FIFO, where it can be processed by a Sobel filter for edge detection, selectable via a button. Synchronization signals (HSYNC, VSYNC) are generated at 9 MHz for VGA output.

In parallel, parabolic guide lines are generated based on a direction value. A distance value is provided by an ultrasonic sensor and computed into the image. These visual elements are combined with the main video into a single 16-bit stream. The result is divided into VGA signals, with synchronization ensuring smooth display. The entire process is continuous, integrating capture, processing, and output in real time.

4. Block Diagram

