

RISC-V Processor

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Project Summary

This project implements a RISC-V core packaged in a microcontroller, featuring the 32-bit base ISA RV32I, four simple peripherals, a 16KB RAM and a 4MB Flash controller.

Implementation

The design was made in Verilog, primarily targeting the von Braun Labs' DevChipBoard, containing the Tang Nano 9k board, running at a base frequency of 27MHz. The RISC-V core is composed of a simple datapath and a multicycle control unit (with up to 4 states).

The core implements the RV32I unprivileged base ISA, enabling the execution of most of the software. The board Flash memory is read in Dual SPI by the controller in enhanced mode, meaning the command doesn't need to be sent at every read, taking roughly 2.5us to read an instruction or (constant) data.

The microcontroller implements a simple memory mapping system, enabling an easy inclusion of peripherals. Four basic peripherals are implemented: Led & Switch, UART, and two OLED displays controllers, all accessible via code in a memory address.

Block Diagram



Visual Resources

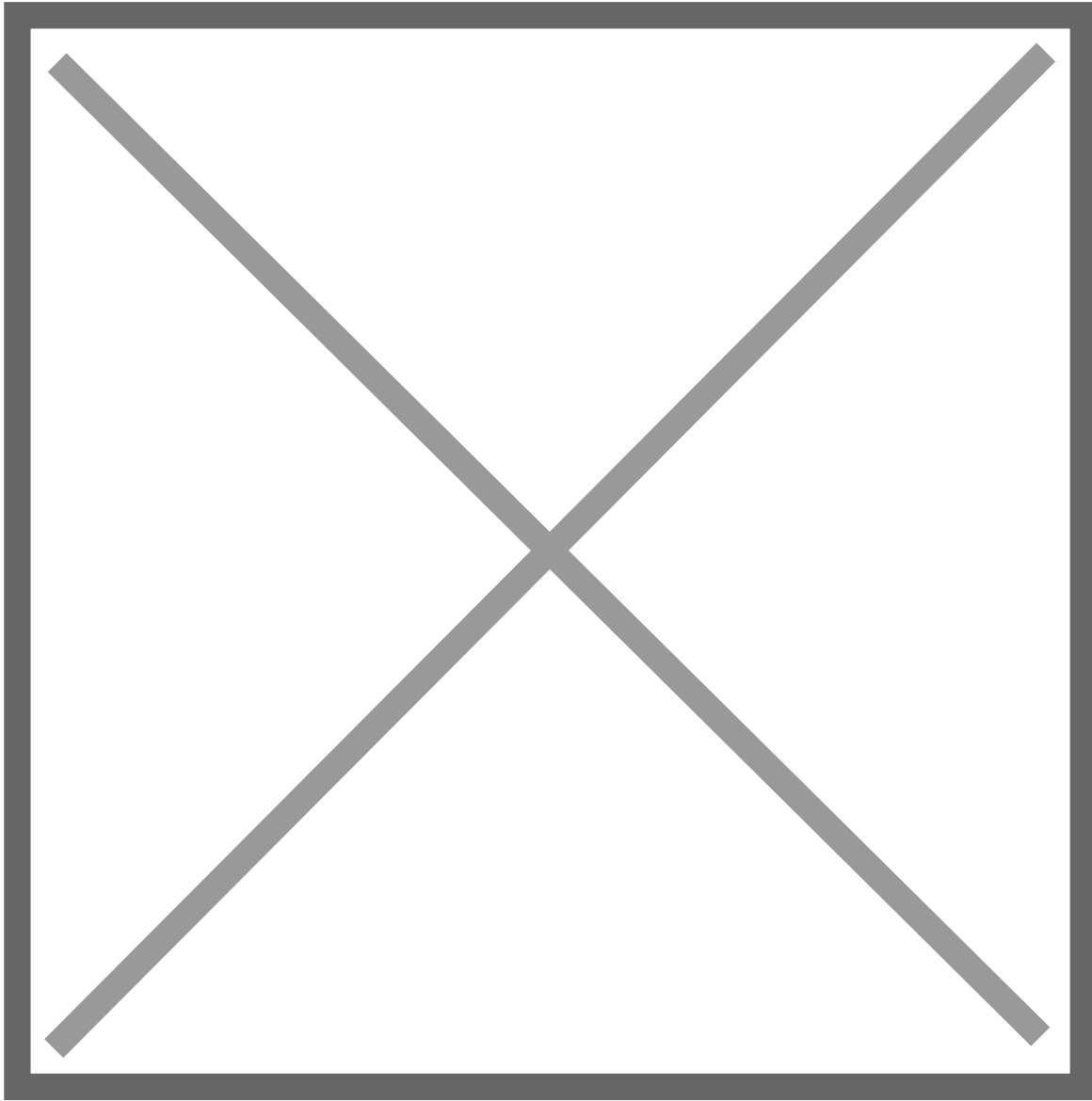


Figure 1: Basic Datapath

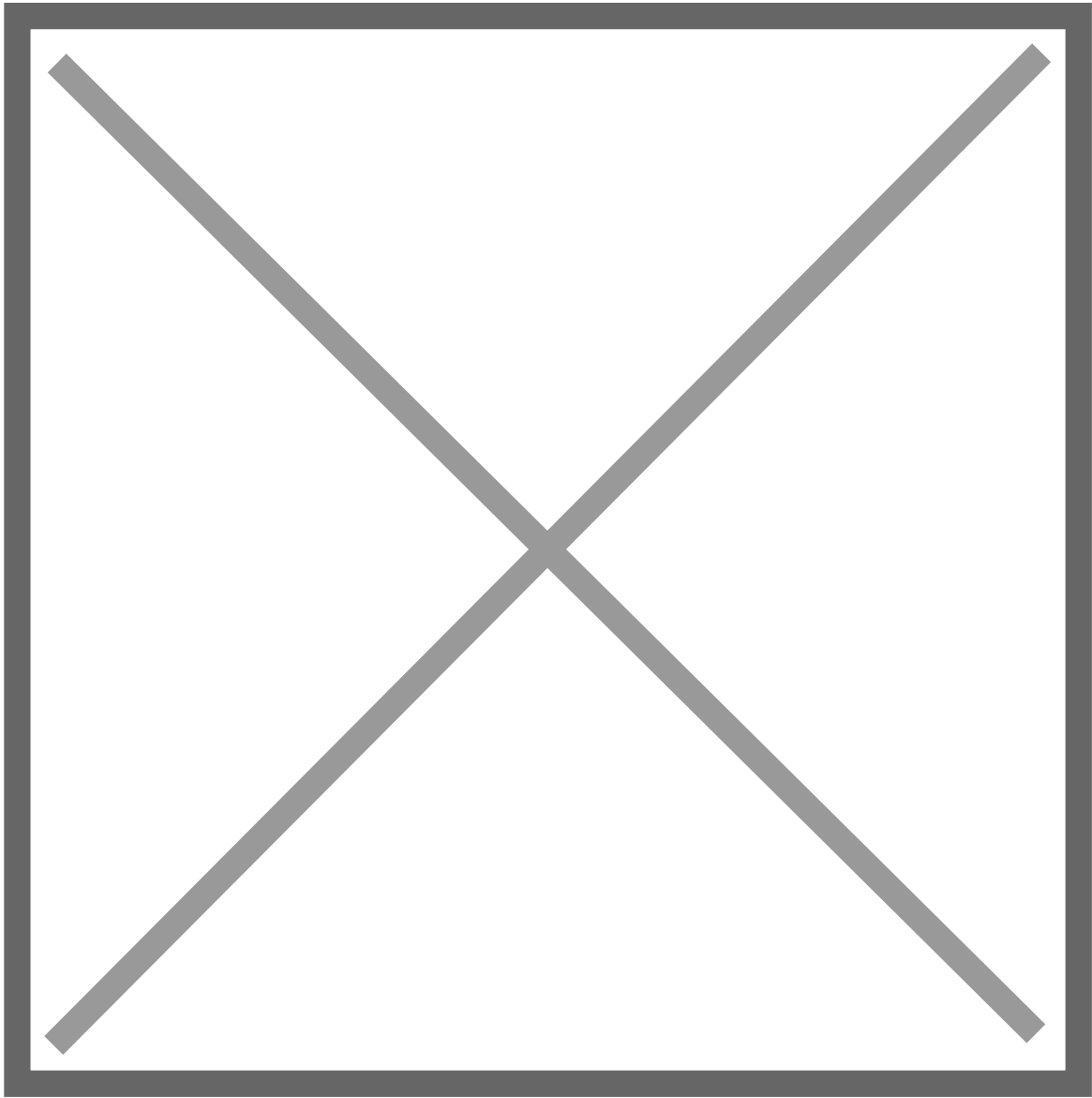


Figure 2: Datapath with Control Signals

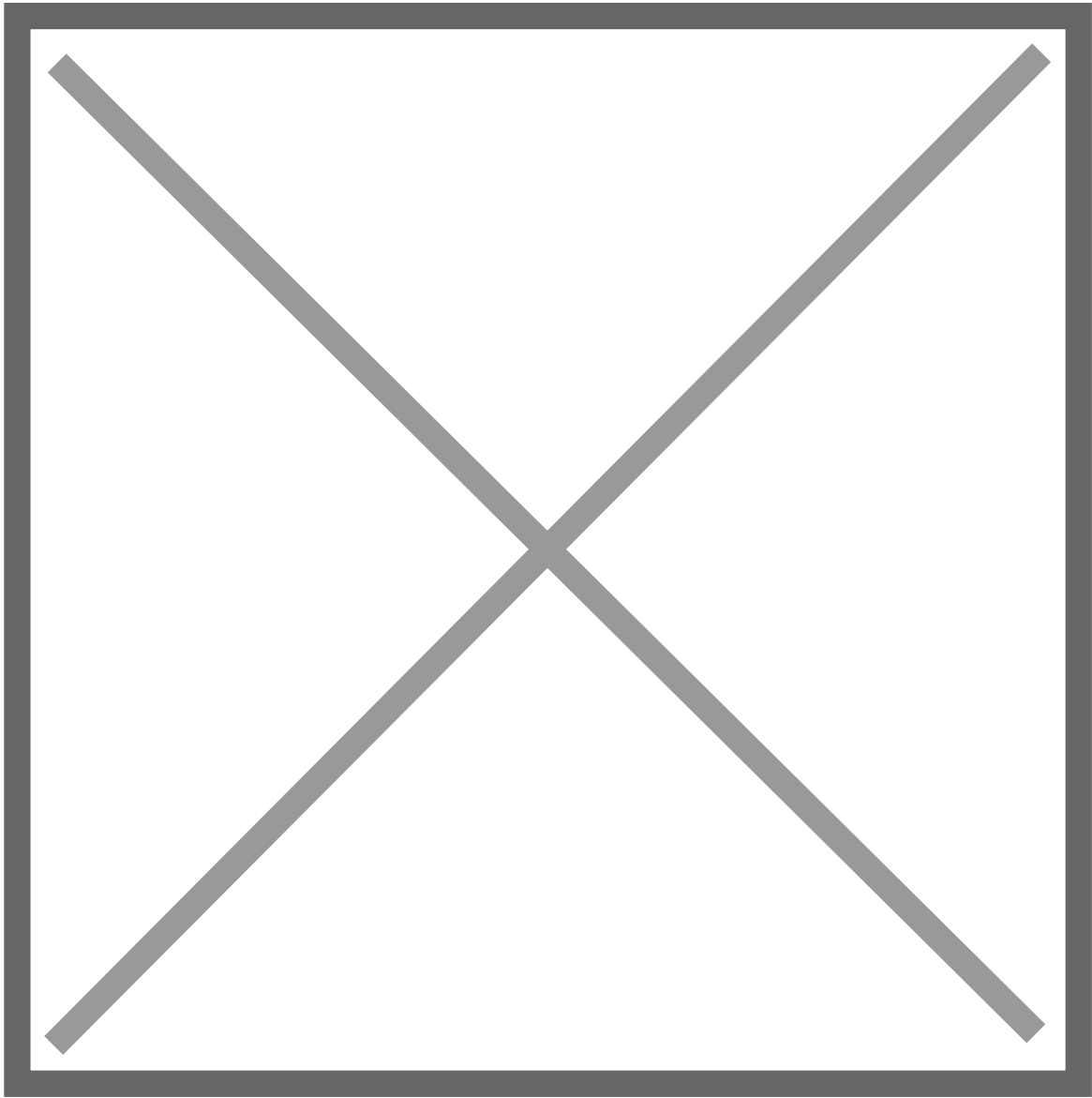


Figure 3: Flash Read Command

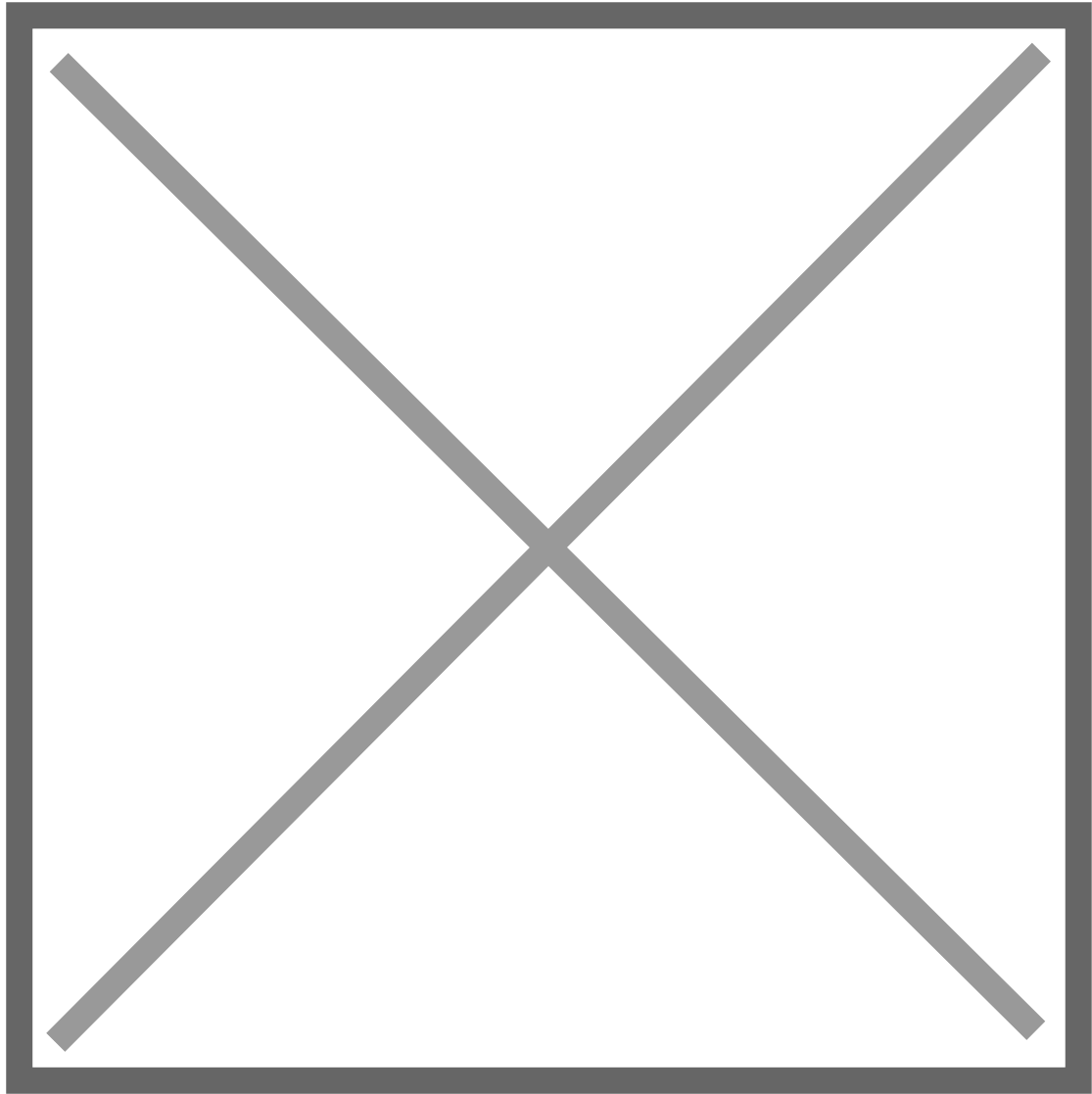


Figure 4: Processor Cycles

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Figure 5: Tang Nano 9k