

Project Simulation

Before programming the FPGA, simulate your project behavior:

- 1. Click on the **Simulate** tab.
- 2. Choose **Advanced Simulation**.
- 3. Click **Menu → Run Iverilog**.
- 4. Observe the main signals:

Signal	Description
acceIX/Y/Z	Sensor data values
value (CORDIC)	Computed tilt angle
valueOut (filter)	Smoothed angle output
active (closeLoop)	Control signal to the servo
pwm	Pulse generated to drive the servo

If errors occur, check the connections and retry.



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