

Hardware Validation

1. Power on both FPGAs.
2. Observe the slave's LEDs—they should display the incrementing byte sent by the master.
3. If the LEDs do not update correctly:
 - Verify the polarity and wiring of `rst_n`.
 - Check connections for `sclk`, `mosi`, and `cs_n` between the boards.
 - Adjust the `CLK_DIV` parameter in `spi_master` for proper timing.
4. (Optional) Use a logic analyzer to probe the SPI lines and verify signal integrity.



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