

Blocks Used in the Project

The project uses the following blocks based on the provided Verilog modules:

- **uart_rx:** Responsible for receiving data from the UART port and indicating when a byte has been completely received.
- **uart_logic_const:** Compares the received byte with a predefined character and toggles an LED state.
- **uart_tx:** Sends data via the UART serial port.
- **Input/Output Pins:**
 - clk: Main system clock
 - uart_rx: UART data input
 - uart_tx: UART data output
 - b0: Reset button
 - led0: Indicator LED



Revision #1

Created 1 May 2025 18:19:41 by Caroline

Updated 1 May 2025 18:20:29 by Caroline